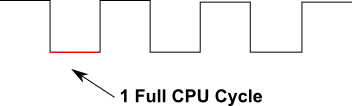
Architecture

Description –

The CPU is built using a 16-bit architecture that includes pipelining – meant to improve the cycle efficiency and protect against certain kinds of hazards. It follows the standard single cycle datapath. What this means is that areas of the CPU ready to execute run on a single clock cycle. This happens during a negative edge of the clock.



The execution will occur within five distinct areas:

* IF – Includes instruction memory and program counter
* ID – Includes registers, instruction controllers, and branching logic
* EX – Includes the ALU
* MEM – Includes the data memory of the program
* WB – Includes the write back logic

Registers are defined based on a 2-bit number with a max of 4 registers. Only 3 of those registers are available for writing. The last one, the 0 register, is read only for the constant 0.